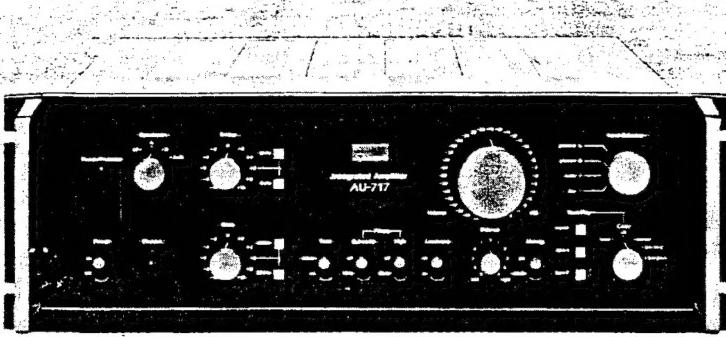


# SERVICE MANUAL

INTEGRATED STEREO AMPLIFIER

**SANSUI AU-517/717**



## SPECIFICATIONS

### AU-517

<b>Power output</b>	W
Min. RMS, both channels driven, from 20 to 20,000 Hz, with no more than 0.025% total harmonic distortion	
65 watts per channel into 8 ohms	
<b>Load impedance</b>	8 ohms
<b>Power bandwidth</b>	20 to 20,000 Hz at or below rated min. RMS power output and total harmonic distortion
<b>Total harmonic distortion (POWER AMP IN)</b>	less than 0.025% at or below rated min. RMS power output
<b>Intermodulation distortion (70 Hz:7 kHz = 4:1 SMPTE method)</b>	less than 0.025%
<b>Frequency response (at 1 watt) (POWER AMP IN)</b>	0 to 200,000 Hz +0 dB -3 dB
<b>RIAA curve deviation (PHONO)</b>	+0.2 dB -0.2 dB (20 to 20,000 Hz)
<b>Damping factor</b>	approximately 60, at 8 ohms load
<b>Input sensitivity and impedance (1 kHz, for rated power output)</b>	
PHONO	2.5 mV/47 kilohms
(Max. input capability: 320 mV at 1 kHz, less than 0.01% harmonic distortion)	
AUX, TAPE	150 mV/47 kilohms
<b>Output level (1,000 Hz)</b>	150mV/47 kilohms
TAPE REC.(pin jack)	150mV/47 kilohms
<b>PRE OUT</b>	1V/47 kilohms
<b>Channel separation (1 kHz, at rated power output)</b>	
PHONO	better than 60 dB
AUX	better than 65 dB
<b>Hum and noise (short-circuit, A-network)</b>	
PHONO	+78 dB
AUX	+100 dB
<b>Controls</b>	
BASS	+10 dB (50 Hz)
TREBLE	+10 dB (15 kHz)
SUBSONIC FILTER	-3 dB (16 Hz), 6 dB/oct
LOUDNESS (-30 dB)	9 dB at 50 Hz 7 dB at 10 kHz

### Power requirements

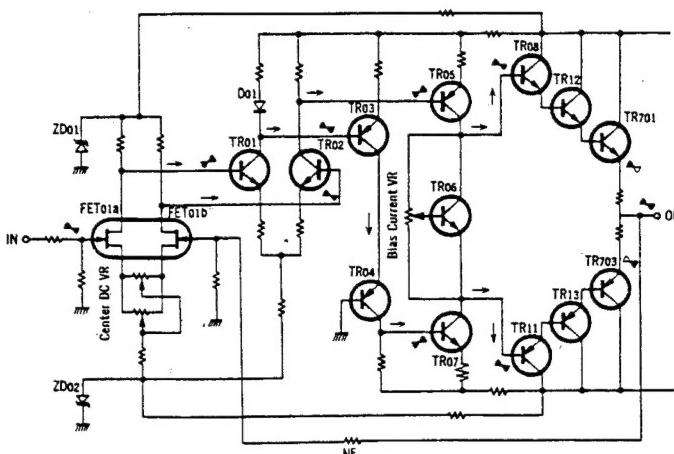
<b>Power voltage</b>	100, 120, 220, 240V (50/60Hz)
	120V (Usable 110 - 130V)
	60 Hz (for U.S.A. & Canada only)
<b>Power consumption</b>	
Maximum consumption	660 watts
Rated consumption	345 watts 420 VA
<b>Dimensions</b>	430 mm (16-15/16") W 168 mm (6-5/8") H 389 mm (15 3/8") D
<b>Weight</b>	16.5 kg (36.4 lbs) net 18.5 kg (40.8 lbs) packed

\* Design and specifications subject to change without notice for improvements.

**Sansui**

SANSUI ELECTRIC CO., LTD.

### 3. ADVANTAGE AND OPERATION OF POWER AMPLIFIER CIRCUITRY SECTION



#### 3-1. Advantage

◇ There is necessity not to decrease the phase response till DC range in order to increase the music signal response of extremely low frequency range. Therefore, this amplifier is employing no capacitors except ones for phase compensation, and has an almost perfect transient characteristics.

◇ The first stage FET (2SK97) is a dual FET of even characteristics and has a large Gm and no-leakage current at normal temperature.

To avoid the influence by temperature drift, such as center voltage (0V) deviation, this FET is used as differential amplifier and operates at cross point which is the optimum point of drain current (at about 3mA) against the temperature drift.

◇ Transistors, TR05 and TR07, the push-pull pre-driver stage functions as current differential amplifier that the stabilized operation can be obtained. In addition, the collector current of these transistors is enough high to make linearity excellent.

◇ Since this Amplifier employs phase advancer circuits [C06, C08, C15, R29, C16 and R30], which have not been frequently used, to compensate the phase characteristics on high frequency range and is also made to have enough

current on each stage to increase the through-rate, the performance on high frequency range is conspicuously improved.

◇ To avoid the voltage deviation, regulated power supply circuit composed of ZD01, ZD02 is employed.

#### 3-2. Operation

The use of differential amplification at first stage dual FET, (FET01, FET02) and connection of the FET to the differential amplifier composed of TR01, TR02, make possible to obtain enough gain and remarkable low distortion.

The output signals of TR01 and TR02 are uniphase. The output signal of TR02 adds to TR05, on the other hand, the output phase of TR01 is inverted by TR03, then, it becomes input signal of TR04 and TR07 which are cascoded connection. The output signals at TR05 and TR07 are inphase that the operation of this stage is push-pull drive and current differential amplification. The power amplifier of the final stage is composed of SEPP (Single Ended Push-Pull) symmetry complementary in 3-stage darlington connection type.

TR09 and TR10 are composing current limiter circuit to protect power transistor from break-down by overload.

### 4. ADJUSTMENTS

#### 4-1. Driver Circuit Board Adjustments (See the picture of top view on page 3.)

Note: 1. Master Volume.....Minimum  
2. Room Temperature.....

3. For adjustment, run the unit for more than 3 minutes after the power is switched on.

STEP	SUBJECT	EQUIPMENT	MEASURE OUTPUT	ADJUST	ADJUST FOR	CONDITION
1.	DC 0V L-CH	DC Volt Meter	Speaker Terminal	F-2721 VR01, VR02	DC 0V±5mV	• Set VR01 and VR02 to center position. • Then, for the purpose of proceeding the accurate adjustment, set the voltage to 0 volt by VR01 first and VR02 next.
2.	DC 0V R-CH	Same as above	Same as above	F-2722 VR01, VR02	DC 0V±5mV	
3.	Bias Current L-CH	Same as above	TP Terminal (+)(-) of F-2721	F-2721 VR03	DC 20mV±1mV	• By turning VR03 counterclockwise, the bias current is decreased gradually.
4.	Bias Current R-CH	Same as above	TP Terminal (+)(-) of F-2723	F-2722 VR03	DC 20mV±1mV	

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7-4. AU-717

